IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): **Shaw** (et al.)
Serial No.: **09/051,263**
Filed: **August 7, 1998**

Attorney Docket: **0081-012**
Examiner: **Li, Aimee J.**
Group Art Unit: **2183**

Title: **RISC Microprocessor Architecture**

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Customer No.: **40972**

This is Box 2 of 2.

The original Information Disclosure Statement (IDS) documents are in Box 1. Copies of Information Disclosure Statement (IDS) documents are in Box 2 for identification purposes.

Box 2 of 2

IDS Document Copies for Identification

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TRANSMITTAL FOR INFORMATION DISCLOSURE STATEMENT

Enclosed for filing in the above-referenced application are the following:

1. Information Disclosure Statement (citing 74 total references);
2. Form PTO-1449 (citing 74 total references);
3. 23 non-United States Patent cited references;
4. Credit Card Form PTO-2038 in the amount of $180.00 (37 C.F.R. §1.17(p)); and
5. Return receipt postcard.

Respectfully Submitted,

Date: 9/18/07

Larry E. Henneman, Jr., Reg. No. 41,063
Henneman & Associates, PLC
714 West Michigan Avenue
Three Rivers, MI 49093

CERTIFICATE OF MAILING (37 CFR 1.8(A))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA, 22313-1450.

Date: 9/18/07

Larry E. Henneman, Jr.

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INFORMATION DISCLOSURE STATEMENT

Pursuant to 37 C.F.R. §1.56, §1.97, and §1.98, Applicants bring the following documents to the Examiner's attention in the above-referenced application:

1. U.S. Patent No. 3,968,501, issued July 6, 1976 to Gilbert;
2. U.S. Patent No. 4,075,691, issued February 21, 1978 to Davis et al.;
3. U.S. Patent No. 4,144,562, issued March 13, 1979 to Cooper;
4. U.S. Patent No. 4,224,676, issued September 23, 1980 to Appelt;
5. U.S. Patent No. 4,236,152, issued November 25, 1980 to Masuzawa et al.;
6. U.S. Patent No. 4,295,193, issued October 13, 1981 to Pomerene;
7. U.S. Patent No. 4,328,557, issued May 4, 1984 to Gastinel;
8. U.S. Patent No. 4,334,268, issued June 8, 1982 to Boney et al.;
9. U.S. Patent No. 4,361,869, issued November 30, 1982 to Johnson et al.;
10. U.S. Patent No. 4,449,201, issued May 15, 1984 to Clark;
11. U.S. Patent No. 4,541,111, issued September 10, 1985 to Takashima et al.;
12. U.S. Patent No. 4,566,063, issued January 21, 1986 to Zolnowsky , et al.;
13. U.S. Patent No. 4,630,195, issued December 16, 1986 to Hester et al.;
14. U.S. Patent No. 4,660,155, issued April 21, 1987 to Thaden et al.;
15. U.S. Patent No. 4,689,581, issued August 25, 1987 to Talbot;
16. U.S. Patent No. 4,691,124, issued September 1, 1987 to Ledzius;
17. U.S. Patent No. 4,710,648, issued December 1, 1987 to Hanamura et al.;
18. U.S. Patent No. 4,714,994, issued December 22, 1987 to Oklobdzija et al.;
19. U.S. Patent No. 4,718,081, issued January 5, 1988 to Brenig;

20. U.S. Patent No. 4,750,111, issued June 7, 1988 to Crosby, Jr., et al.;
21. U.S. Patent No. 4,763,297, issued August 9, 1988 to Uhlenhoff;
22. U.S. Patent No. 4,766,567, issued August 23, 1988 to Kato;
23. U.S. Patent No. 4,803,621, issued February 7, 1989 to Kelly;
24. U.S. Patent No. 4,805,091, issued February 14, 1989 to Thiel et al.;
25. U.S. Patent No. 4,890,225, issued December 26, 1989 to Ellis, Jr. et al.;
26. U.S. Patent No. 4,914,578, issued April 3, 1990 to MacGregor et al.;
27. U.S. Patent No. 4,931,748, issued June 5, 1990 to McDermott;
28. U.S. Patent No. 4,933,835, issued June 12, 1990 to Sachs et al.;
29. U.S. Patent No. 4,942,553, issued July 17, 1990 to Dalrymple et al.;
30. U.S. Patent No. 4,979,102, issued December 18, 1990 to Tokuume;
31. U.S. Patent No. 4,989,133, issued January 29, 1991 to May et al.;
32. U.S. Patent No. 5,021,991, issued June 4, 1991 to MacGregor et al.;
33. U.S. Patent No. 5,081,574, issued January 14, 1992 to Larson et al.;
34. U.S. Patent No. 5,097,437, issued March 17, 1992 to Larson;
35. U.S. Patent No. 5,103,499, issued April 7, 1992 to Miner et al.;
36. U.S. Patent No. 5,134,701, issued July 28, 1992 to Mueller et al.;
37. U.S. Patent No. 5,146,592, issued September 8, 1992 to Pfeiffer et al.;
38. U.S. Patent No. 5,148,385, issued September 15, 1992 to Frazier;
39. U.S. Patent No. 5,226,147, issued July 6, 1993 to Fujishima et al.;
40. U.S. Patent No. 5,237,699, issued August 17, 1993 to Little;
41. U.S. Patent No. 5,325,513, issued June 28, 1994 to Tanaka;
42. U.S. Patent No. 5,353,427, issued October 4, 1994 to Fujishima et al.;
43. U.S. Patent No. 5,379,438, issued January 3, 1995 to Bell et al.;
44. U.S. Patent No. 5,421,000, issued May 30, 1995 to Fortino et al.;
45. U.S. Patent No. 5,459,846, issued October 17, 1995 to Hyatts;
46. U.S. Patent No. 5,530,890, issued June 25, 1996 to Moore et al.;
47. U.S. Patent No. 5,604,915, issued February 18, 1997 to Moore et al.;
48. U.S. Patent No. 5,659,703, issued August 19, 1997 to Moore et al.;
49. U.S. Patent No. 5,784,584, issued July 21, 1998 to Moore et al.;
50. U.S. Patent No. 5, 809,336, issued September 15, 1998 to Moore et al.;

51. U.S. Patent No. 6,598,148, issued July 22, 2003 to Moore et al.;

52. JP Patent Doc. JP SHO 61(1986)-127228, dated June 14, 1984 by Hitachi Ltd.; (Japanese language abstract included)

53. EP Patent Doc. EP 85105578.0, dated November 18, 1984 by INMOS Limited;

54. "Engineering Data IMS T414M Transputer"; August 1987, pp. 1-39.;

55. "TLCS-42,47,470 User's Manual "; April 1986, pp. I. MCU47-117 through 203.;

56. "SM550/SM551/SM552 4-bit Microcomputer (Controller)"; 1982-1983, pp. 41-108.;

57. "Microprocessors in Brief"; Robert C. Stanley, *IBM J. Res. Develop.*, Vol. 29, No. 2, March 1985, pp. 115-116.;

58. "Microprocessor System Bus"; *IEEE Std 796-1983,* December 1983, pp. 9-46.;

59. "Introduction to VLSI Systems"; *Mead & Conway*, 1980, pp. 1-429.;

60. MOSTEK CORP., "Mostek 1981 3870/F8 Microcomputer Data Book", February 1981, pp. III-76 through III-77, III-100 through III-129, and VI-1 through VI-11.;

61. MOSTEK CORP., Advertisement, *EDN*, November 20, 1976.;

62. UNITED TECHNICAL PUBLICATIONS, IC Master, 1980, pp. 1 and 2016-2040.;

63. GUTTAG, K. M., "The TMS34010: An Embedded Microprocessor", *IEEE Micro*, vol. 8, no. 3, May 1988, pp. 39-52;

64. HITACHI AMERICA LTD., "8-Bit Single-Chip Microcomputer Data Book", July 1985, Table of Contents and pp. 251-279.;

65. "TPL Web Site, www.tplgroup.net/patents/index.php", August 3, 2006, 3 pgs.;

66. "The IBM System/ 360 Model 91: Machine Philosophy and Instruction-Handling.", D.W. Anderson, *IBM Journal*, January 1967, pp. 11-20.;

67. "GE 625/635 Programming Reference Manual", *General Electric*, July 1964, pp. I-1, II-3, II-127-128, III-62.;

68. "Clipper 32-bit Microprocessor: Introduction to the Clipper Architecture", March 1986, pp. 2-1 through 2-8.;

69. "IBM RT PC Romp", Simpson & Hester, *IBM Systems Journal*, Vol. 26, No. 4, 1987, pp. 60, 347-56.;

70. "i860 64-bit Microprocessor: Advance Information", February 1989, pp. 7-27.;

71. "Intel's 80960: An Architecture Optimized for Embedded Control", David P. Ryan, *IEEE Micro*, June 1988, pp. 64-72; and

72. "IBM RT Personal Computer Technology", *IBM Corp.*, 1986, p. 60.

73. "MIPS: A Microprocessor Architecture", John Hennessy et al., *IEEE*, 1982, pp. III – 62.

74. "Multi-Microprocessor Systems", APIC Studies in Data Processing, Chptr. 1, no. 18, pp.1-23 (1983).

A PTO form 1449 listing these documents is enclosed.

The relevance of the attached references is that they were cited in other patent applications of Applicants related to similar technology.

Citation of the above documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made, other than as described above; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. §1.56(b).

This information disclosure statement is filed after the mailing of an office action on the merits, but before the mailing of a final action. Therefore, pursuant to 37 CFR §1.97(c), a PTO Form-2038 for the fee set forth in 37 CFR §1.17(p) is enclosed.

Respectfully Submitted,

Date: 9/18/07

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Larry E. Henneman, Jr.

THE STAMP OF THE UNITED STATES PATENT AND TRADEMARK OFFICE HEREON ACKNOWLEDGES RECEIPT OF THE FOLLOWING:

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Documents Received:

1. IDS Transmittal Letter (1 page);
2. Information Disclosure Statement (4 pages);
3. Form PTO-1449 (4 pages);
4. 23 Non- U.S. Patent References; and
5. Credit Card Form 2038 in the amount of $180.00 (37 C.F.R. §1.17(p)).

Date: September 18, 2007
Initials: LEH:cmc

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